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| | |
|--------------|-----------------------|
| Re Applic of | Carl J. Radens et al. |
| Docket No. | FIS920000011US2 |
| Serial No. | 09/873,537 |
| Filing Date | June 4, 2001 |
| Attorney | Steven Capella |

Attached: Transmittal of Appeal Brief, and Appeal Brief

PLEASE DELIVER TO:

EXAMINER: Monica Lewis

ART UNIT: 2812

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Phone: 845-894-2580

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
FIS920000011US2

In Re Application Of:

Carl J. Radens et al.

Application No.

09/873,537

Filing Date

June 4, 2004

Examiner

Monica Lewis

Customer No.

32074

Group Art Unit

2812

Confirmation No.

4948

Invention: Dual Damascene Anti-Fuse with Via Before Wire

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on August 8, 2004

The fee for filing this Appeal Brief is: \$340.00

- ☐ A check in the amount of the fee is enclosed.
- ☒ The Director has already been authorized to charge fees in this application to a Deposit Account.
- ☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 09-0458 FI-308
- ☐ Payment by credit card. Form PTO-2038 is attached.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.


Signature

Dated: 10/18/04

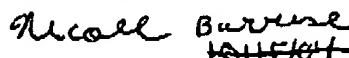
Steven Capella
Registration No. 33,086
Telephone No. 845-894-3669
Fax No. 845-892-6363

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Nicola Barrese 10-15-04
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit 2822

| | | |
|---------------------------------|---|-------------------------|
| <u>In re application of</u> | : | October 18, 2004 |
| Carl J. Radens et al. | : | Examiner: Monica Lewis |
| Serial No. : 09/873,537 | : | Confirmation No.: 4948 |
| Filed: June 4, 2001 | : | IBM Corporation |
| | : | Dept. 18G/Bldg, 300-482 |
| Title: DUAL DAMASCENE ANTI-FUSE | : | 2070 Route 52 |
| WITH VIA BEFORE WIRE | : | Hopewell Junction, NY |
| | : | 12533-6531 |

APPEAL BRIEF

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Final Rejection of claims 22-30. A correct copy of the claims is attached in the Appendix.

Real Party in Interest

The real parties in interest are International Business Machines Corporation per an assignment recorded in the US Patent and Trademark Office at Reel/Frame: 011199/0187 on October 16, 2000 and Infineon Technologies North America Corp. per an assignment recorded in the US Patent and Trademark Office at Reel/Frame: 011198/0060 on October 16, 2000.

Related Appeals and Interferences

None.

Status of Claims

Claims 22-30 are pending.

Status of Amendments

No amendments after Final Rejection have been submitted.

Summary of the Claimed Subject Matter

The invention centers on novel interconnect structures having an anti-fuse formed as a layer having openings that define via locations. The structures of the invention advantageously incorporate anti-fuses at reduced manufacturing cost. See the specification at page 4, lines 10-29, Figures 2e, 2f and 3.

Grounds of Rejection to be Reviewed on Appeal

1. Claims 22, 23, 26, 27, 29 and 30 are rejected under 35 USC 102(b) as being anticipated by Dixit et al. (US Pat. 5233217).
2. Claim 24 is rejected under 35 USC 103(a) as being obvious over Dixit et al. (US Pat. 5233217) in view of Chang (US Pat. 5807786).

3. Claim 25 is rejected under 35 USC 103(a) as being obvious over Dixit et al. (US Pat. 5233217) in view of Go et al. (US Pat. 5592016).
4. Claim 28 is rejected under 35 USC 103(a) as being obvious over Dixit et al. (US Pat. 5233217) in view of Shroff et al. (US Pat. 6515343).

Argument

1. **Claims 22, 23, 26, 27, 29 and 30 are rejected under 35 USC 102(b) as being anticipated by Dixit et al. (US Pat. 5233217).**

Dixit et al. (US Pat. 5233217) discloses conventional anti-fuse structures where the antifuse material is deposited into formed vias. Dixit et al. does not disclose or suggest or suggest an antifuse layer which defines interconnect via locations and is also an antifuse. Appellants specifically note that layer 11 of Figure 1 G does not form part of an antifuse path.

For these reasons, appellants submit that Dixit et al. does not anticipate the appealed claims.

2. **Claim 24 is rejected under 35 USC 103(a) as being obvious over Dixit et al. (US Pat. 5233217) in view of Chang (US Pat. 5807786).**

Dixit et al. (US Pat. 5233217) discloses conventional anti-fuse structures where the antifuse material is deposited into formed vias. Dixit et al. does not disclose or suggest or suggest an antifuse layer which defines interconnect via

locations and is also an antifuse. Appellants specifically note that layer 11 of Figure 1 G does not form part of an antifuse path.

Chang et al. (US Pat. 5807786) discloses antifuse structures using various antifuse materials. Chang et al. does not disclose or suggest or suggest an antifuse layer which defines interconnect via locations and is also an antifuse. Appellants submit that the combination of the teachings of Dixit et al. and Chang et al. would still result in a structure lacking antifuse layer which defines interconnect via locations and is also an antifuse.

For these reasons, appellants submit that the combination of Dixit et al. with Chang et al. does not render the appealed claim obvious.

3. **Claim 25 is rejected under 35 USC 103(a) as being obvious over Dixit et al. (US Pat. 5233217) in view of Go et al. (US Pat. 5592016).**

Dixit et al. (US Pat. 5233217) discloses conventional anti-fuse structures where the antifuse material is deposited into formed vias. Dixit et al. does not disclose or suggest or suggest an antifuse layer which defines interconnect via locations and is also an antifuse. Appellants specifically note that layer 11 of Figure 1 G does not form part of an antifuse path.

Go et al. (US Pat. 5592016) discloses anti-fuse structures which are located above or below vias. Go et al. does not disclose or suggest or suggest an antifuse layer which defines interconnect via locations and is also an antifuse. Appellants submit that the combination of Go et al. with Dixit et al. would only result in conventional antifuses of Go et al. being formed in combination with damascene interconnect structures.

For these reasons, appellants submit that the combination of Dixit et al. with Go et al. does not render the appealed claim obvious.

4. **Claim 28 is rejected under 35 USC 103(a) as being obvious over Dixit et al. (US Pat. 5233217) in view of Shroff et al. (US Pat. 6515343).**

Dixit et al. (US Pat. 5233217) discloses conventional anti-fuse structures where the antifuse material is deposited into formed vias. Dixit et al. does not disclose or suggest or suggest an antifuse layer which defines interconnect via locations and is also an antifuse. Appellants specifically note that layer 11 of Figure 1 G does not form part of an antifuse path.

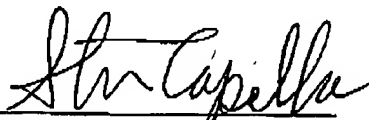
Shroff et al. (US Pat. 6515343) discloses various antifuse structures and materials. Shroff et al. does not disclose or suggest or suggest an antifuse layer which defines interconnect via locations and is also an antifuse. Appellants submit that the combination of Shroff et al. with Dixit et al. would only result in conventional antifuses of Shroff et al. being formed in combination with damascene interconnect structures.

For these reasons, appellants submit that the combination of Dixit et al. with Shroff et al. does not render the appealed claim obvious.

Conclusion

Based on the above arguments, appellants submit that the present claims are patentable over the prior art of record that the rejections under 35 USC 102(b) and 35 USC 103(a) should be reversed.

Respectfully submitted,
Carl J. Radens et al.

By 
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